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09/595,036	06/15/2000	Ted Scott Rakel	10992563-1	9158

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EXAMINER	
FERRIS III, FRED O	
ART UNIT	**PAPER NUMBER**
2128	2

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/595,036	Applicant(s) RAKEL ET AL.	
	Examiner Fred Ferris	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. *Claims 1-20 have been presented for examination. Claims 1-20 have been rejected by the examiner.*

Claim Interpretation

2. *The claimed invention is disclosed to be a method using circuit simulation for determining the DC margin (one and zero margin) of a simulated latch circuit and associated path elements using worst case DC analysis of the pull-up/pull-down signal path to determine a weighted (accumulated) resistance for elements along a particular signal path. The invention appears to rely on the use of features inherent to the commercially available SPICE circuit simulation program, well-known DC analysis techniques, and well-known weighting techniques in performing the simulation of the latch circuit and associated path analysis.*

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one

skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification does not disclose the specific steps involved in the circuit simulation for determining the one margin or the zero margin in performing the DC analysis of the simulated latch circuit and related elements. No algorithms or flow charts have been presented which specifically disclose how the margins are determined, or how the latch circuit and path elements are simulated. Merely stating the one margin, for example, is the difference V_{trip} of the forward inverter and the worst case pull-up input level at the latch (specification page 2, line 2) does not cure this deficiency. Accordingly, a skilled artisan would be at odds to determine how to realize the claimed method for determining the DC margin of a latch circuit based on the information provided in the disclosure without undue experimentation.

4. Claims 1-20 are also rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Specifically, claims 1-20 are drawn to limitations that appear to rely entirely on inherent features of the MicroSim Spice program. The specification does not provide a written description of the specific steps involved in the circuit simulation for determining the one margin or the zero margin in performing the DC analysis of the simulated latch

circuit and related elements. No algorithms or flow charts have been presented which specifically disclose how the margins are determined, or how the latch circuit and path elements are simulated. Merely stating the one margin, for example, is the difference V_{trip} of the forward inverter and the worst case pull-up input level at the latch (specification page 2, line 2) does not cure this deficiency. Accordingly, a skilled artisan would be at odds to determine how to realize the claimed method for determining the DC margin of a latch circuit from the written description provided in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Independent claims 1, 8, and 15 are drawn to:
Method, computer code, and simulated circuit for determining DC margin of a latch by:
Performing simulation to determine trip voltage (threshold) of forward inverter of latch
Performing worst case pull-up path simulation to determine one margin of latch
Performing worst case pull-down path simulation to determine zero margin of latch

5. *Claims 1, 8, and 15 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by U.S. patent 6,292,766 issued to Mattos et al.*

Per claims 1, 8, and 15: Mattos teaches the use of the Spice circuit simulation program (and file conversion) in performing DC analysis of circuit path elements (latches, inverters, drivers, etc.) to determine simulated circuit element parameters including threshold (trip) voltages, pull-up path analysis, pull-down path analysis, and

provides the facilities to determine the differences between threshold and input/output voltages between circuit elements and pull-up/pull-down path signal levels (i.e. one and zero margins). (Abstract, Summary of Invention, CL12-L45-67, CL13-L13-31, Figs. 1-11, 14-18, especially Fig. 18)

6. Claims 1, 8, and 15 are also rejected under 35 U.S.C. 102(b) as being clearly anticipated by "MicroSim PSpice A/D Reference Manual", MicroSim Corporation, Version 8.0, June 1997.

Per claims 1, 8, and 15: MicroSim discloses the PSpice circuit simulation program for creating, simulating, and analyzing circuit designs and performing DC analysis of circuit path elements to determine the differences between threshold and input/output voltages between circuit elements and pull-up/pull-down path signal levels (i.e. one and zero margins). (Overview, Glossary, pp. xix-xxiv, 1-2 to 1-3, 4-2 to 4-12)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 2-7, 9-14, and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over "MicroSim PSpice A/D Reference Manual", MicroSim Corporation, Version 8.0, June 1997 in view of "Fast generation of statistically-based worst-case modeling of on-chip interconnect, N. Chang et al", Computer Design: International Conference on VLSI in Computers and Processors, IEEE 1997.

Per dependent claims 2-7, 9-14, and 16-20: Dependent claims 2-7, 9-14, and 16-20 are drawn to the use of a weighting function in analyzing the signal paths. As cited above, MicroSim discloses the PSpice circuit simulation program for creating, simulating, and analyzing circuit designs and performing DC analysis of circuit path elements to determine the differences between threshold and input/output voltages between circuit elements and pull-up/pull-down path signal levels (i.e. one and zero margins). (Overview, Glossary, pp. xix-xxiv, 1-2 to 1-3, 4-2 to 4-12) Since the intended commercial use the MicroSim SPICE program is for circuit simulation and analyzing of circuit designs, and since SPICE includes inherent DC and path analysis of circuit elements, it would have been an obvious choice for a skilled artisan to use to realize the claimed method simulating a latch circuit and determining the DC margin of the latch circuit.

MicroSim does not explicitly teach the use of weighting in analyzing the signal paths.

Chang discloses the use of weighting in analyzing the signal paths in a circuit design. Chang teaches the use of weighting of both resistance and capacitance and worst-case analysis of elements in a circuit path. The examiner notes that the weighting the path elements by length, width, resistance, etc. is well-known in the art and commonly used commercially available circuit layout programs (See Abstracts: U.S. 6,542,509, U.S. 5,654,898, U.S. 5,359,538, for example). (Abstract, Introduction, Sections 3-5, Figs. 1, 2)

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of the MicroSim PSpice circuit simulation program for creating, simulating, and analyzing circuit designs, with the teachings of Chang relating to the use of weighting in analyzing the signal paths in a circuit design, to realize the claimed invention. An obvious motivation exists since this area of technology is highly competitive with many types of circuit simulators available in the market place and large amounts of money being spent in product development and improvement. (i.e. SPICE, MATLAB, APLAC, etc., for example) Accordingly, a skilled artisan would have made an effort to become aware of what capabilities had already been developed in the market place and, hence, would have been motivated to modify the teachings of MicroSim PSPICE with the teachings of Chang in order to reduce development time and cost.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 5,359,538 issued to Hui et al teaches weighting in circuit path analysis.

U.S. Patent 6,542,509 issued to Giroux teaches weighting in circuit path analysis.

"A Simulation Program Emphasized on DC Analysis of VLSI Circuits; SAMOC", Y. Jan, IEEE 0-7803-5510-0-5/99, IEEE May 1999 teaches circuit simulation and DC analysis.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 703-305-9670 and whose normal working hours are 8:30am to 5:00pm Monday to Friday.

Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 703-305-3900.

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